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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,750	02/04/2004	Koichi Yamada	P18129	5683

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,750	YAMADA ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/26/2009, 06/23/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/26/2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, and 10-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Zalewski et al (U.S. Patent # 6,260,068 B1), herein referred to as Zalewski.

4. As per claim 1, Zalewski discloses a method comprising: in a processor based system (See figure 1: A processor based system is illustrated) where a plurality of logical processors (See figure 1: The figure shows at least 16 processors) share processor execution resources (See column 7, lines 53-55: Resources can be shared), in response to a first logical processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks (column 32, lines 39-45, When a resource is not needed by a processor, then the processor resource is scheduled to enter an idle state.), making a processor execution resource previously reserved for the first logical processor available to any of the plurality of logical processors (column 32, lines 39-45, In response to the processor entering an idle state, the resource is returned to the unassigned pool of resources and available to the processors.).

5. As per claim 2, Zalewski discloses further comprising reserving the processor execution resource for the first processor in response to the first processor being scheduled to execute a task (See column 4, lines 62-65 and 32, lines 39-45: System will lock up resources if needed by a processor).

6. As per claim 3, Zalewski discloses wherein each of the plurality of processors is a logical processor of the processor based system (See figure 1).

7. As per claim 4, Zalewski discloses wherein the first processor being scheduled to enter an idle state further comprises the first processor executing a processor instruction requesting the first processor to enter an idle state (See column 20, lines 7-17, column 32, lines 39-45).

8. As per claim 5, Zalewski discloses wherein making the processor execution resource previously reserved for the first processor available to any of the plurality of processors further comprises releasing the processor execution resource into a common pool of processor execution resources (column 32, lines 39-45).

9. As per claim 10, Zalewski teaches a processor comprising:a plurality of logical processors (See figure 1: The figure shows at least 16 processors); and logic to execute an instruction set which when executed by a first logical processor (See column 31, lines 52-55), cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors (column 32, lines 39-45: Zalewski teaches the migration of resources which makes resources available to other processors) in response to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks (column 32, lines 39-45, column 32, lines 39-45, When a resource is not needed by a processor (i.e due to a lack of scheduled tasks that require the resource), then the processor resource is scheduled to enter an idle state.).

10. As per claim 11, Zalewski discloses wherein to the first logical processor being scheduled to enter an idle state further comprises the first processor executing a processor instruction requesting the first logical processor to enter an idle state (See column 4, lines 62-65: An idle states does exist in the system, 32, lines 39-45).

11. As per claim 12, Zalewski discloses wherein causing the first logical processor to make the processor execution resource previously reserved for the first logical processor available to a second logical processor further comprises releasing the processor execution resource into a common pool of processor execution resources accessible from the second logical processor (See column 29, lines 39-44, column 32, lines 39-45).

12. As per claim 13, Zalewski discloses wherein the processor execution resource previously reserved for the first logical processor further comprises the processor execution resource previously statically allocated to the first logical processor; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource (See column 29, lines 39-44, column 32, lines 39-45).

13. As per claim 14, Zalewski discloses wherein the processor execution resource previously reserved for the first logical processor further comprises the processor execution resource previously statically allocated to the first logical processor (See column 29, lines 39-44, column 32, lines 39-45); and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises the first processor unlocking the processor execution resource (See column 29, lines 39-44, column 32, lines 39-45).

14. As per claims 15-19, Zalewski discloses the limitations of the claims for similar reasoning to above rejections of claims 10-14. The difference between these two sets of claims is claims 15-19 are directed to a system, which Zalewski discloses in column 5, lines 46-50. Claim 15 also has the added limitation of wherein the system comprises firmware (See figure 3: The hardware root is the firmware) to schedule the first logical processor to enter an idle state (column 32, lines 39-45, When a resource is not needed by a processor, then the processor resource is scheduled to enter an idle state. See column 11, lines 10-13: When an idle state is entered into the firmware); and a bus to interconnect the firmware and the processor (See figure 3: The hardware root is connected to the processor through a bus).

15. As per claims 20-24, Zalewski discloses the limitations of the claims for similar reasoning to above rejections of claims 1-5. The difference between these two sets of claims is claims 20-28 are directed to a machine accessible medium having stored thereon data which when accessed by a machine causes the machine to perform a method, which Zalewski discloses in column 31, lines 52-55.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6-9, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zalewski et al (U.S. Patent # 6,260,068 B1), herein referred to as Zalewski.

18. As per claim 6, Zalewski teaches the method of claim 2 (See 35 USC 102(b) rejection of claim 5). Zalewski dos not teach wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Zalewski to include a wake up signal since a wake up signal is necessary to indicate to a processor that it is no longer waiting or else the processor would permanently wait and no further processes would occur. Zalewski teaches waiting and coming out of a waiting state (See column 28, lines 44-51, column 32, lines 39-45), but does not teach the intermediate wake up signal which would be obvious to implement.

19. As per claim 7, Zalewski discloses wherein the processor execution resource previously reserved for the first processor further is statically allocated to the first processor (column 32, lines 39-45: If a resource is released, it means it must have been previously owned); and
wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource (column 32, lines 39-45).

20. As per claim 8, Zalewski discloses wherein the processor execution resource previously reserved for the first processor is locked by the first processor (column 32, lines 39-45); and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises the first processor unlocking the processor execution resource (column 32, lines 39-45).

21. As per claim 9, Zalewski teaches the method of claim 5. Zalewski does not teach a translation lookaside buffer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Zalewski to include the common pool of processor execution resources comprises a translation lookaside buffer and the processor execution resource is a translation cache entry from the translation lookaside buffer. A translation lookaside buffer is well known and

commonly used in the art. Zalewski already teaches the mapping of a database to local memory, which is similar functionality of a TLB (See figure 8). A TLB could be used in conjunction of the database and eliminate the need for the mapping of the database to memory by using a TLB.

22. As per claims 25-28, Zalewski teaches-the limitations for the similar reasoning as for claims 6-9.

Response to Arguments

23. Applicant's arguments filed 05/26/2009 have been fully considered but they are not persuasive.

24. Applicant argues that novelty/rejection of the claims, in substance that:

A) "Zalewski does not disclose, teach nor suggest 'a plurality of logical processors'" (page 10 or reply)

25. These arguments are not found persuasive for the following reason:

Regarding point A), Zalewski has taught a plurality of processors (see Fig. 1; plurality of CPUs). Because these processors are physical processors, they are logical processors. That is, they both logically and physically represent a processor. Therefore, Zalewski has taught "a plurality of logical processors" as claimed. If the applicant intends for the claims to be read as consisting of only one physical processor that implements multiple logical processors, then the claims should be amended to require such a reading.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

Benjamin P Geib
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